Biyani's Think Tank

Concept based notes

Physics

(BCA-I)

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Preface

I am glad to present this book, especially designed to serve the needs of the students. The book has been written keeping in mind the general weakness in understanding the fundamental concepts of the topics. The book is self-explanatory and adopts the "Teach Yourself" style. It is based on question-answer pattern. The language of book is quite easy and understandable based on scientific approach.

This book covers basic concepts related to the microbial understandings about diversity, structure, economic aspects, bacterial and viral reproduction etc.

Any further improvement in the contents of the book by making corrections, omission and inclusion is keen to be achieved based on suggestions from the readers for which the author shall be obliged.

I acknowledge special thanks to Mr. Rajeev Biyani, *Chairman* & Dr. Sanjay Biyani, *Director* (*Acad.*) Biyani Group of Colleges, who are the backbones and main concept provider and also have been constant source of motivation throughout this Endeavour. They played an active role in coordinating the various stages of this Endeavour and spearheaded the publishing work.

I look forward to receiving valuable suggestions from professors of various educational institutions, other faculty members and students for improvement of the quality of the book. The reader may feel free to send in their comments and suggestions to the under mentioned address.

Author

Content

Chapter 1

Review of Concepts

Q.1. What is positive and negative logic.

Sol. Logics 1 and O are generally represented by voltage levels. In a time logic system, the highest level of voltage depicts 1 and lowest state depicts O. 111^{ly}, in – ive logic system, the highest level of voltage represent 08 highest level 1. They are just opposite of each other. To convert a + ive logic system to negative logic system and vice versa, we just have to replace all O's with 1's and 1's with O's.

Q.2. Which are the basic Boolean logic operations?

Sol. The basic Boolean operation are

(1) AND operation- The Logical and operation of 2 boolean variables A & B is given as.

Y = A 0 B

The symbol for this operation is multiplication sign. (O). The truth table is given below:-

I/P		O/P
A	B	Y = A.B
0	0	0
0	1	0
1	0	0
1	1	1

(2) OR Operation: The Logical OR operation of 2 boolean variables A & B is given as:

$$Y = A + B$$

The symbol for this operation is addition sign (+).

The Truth table is shown below-

I/P		O/P
A	B	Y = A+B
0	0	0
0	1	1
1	0	1
1	1	1

(3) NOT Operation: Its also called as inversion or complement of the variable. This operation converts the logical 1 to 0 and 0 to 1. Its represented as:

$$Y = \overline{A} \; or \; Y = NOT \; A \; or \; Y = 7A$$

(4) XOR Operation: The XOR operation is known as exclusive OR operation. Its represented by:

$$Y = A \oplus B$$

The truth table is shown below:

I/P		O/P
A	B	Y = A+B
0	0	0
0	1	1
1	0	1
1	1	0

The XOR function can be also written as:

$$Y = A\overline{B} + \overline{A}B = A \oplus B$$

EXNOR Operation: Its known as exclusive –NOR gate. Its represented it.

$$Y = \overline{A \oplus B}$$

The truth table for it is as following.

I/P		O/P
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Q.3. Explain the basic Laws of Boolean algebra and properties of Boolean algebra.

Sol. Logical expressions can be expressed and minimized mathematically using the rules, laws and theorms of Boolean algebra.

(i) Boolean Addition: It is nothing but logical OR operation..

(ii) Boolean multiplication: Its nothing but logical AND operation.

Properties :

(1) Commutative property: Boolean addition is commutative.

A+B = B+A

Boolean Multiplication is also commutative.

$A.B = B.A$

(2) Associative Law: Boolean addition is associative.

$A + (B + C) = (A + B) + C$

Boolean multiplication is also associative.

$A.(B.C) + (A.B).C.$

(3) Distributive Law: Boolean addition is distributive as well.

$A + BC = (A + B)(A + C)$

Boolean multiplication is distributive.

$A.(B + C) = A.B + A.C.$

Some other Laws :

(1) $A + AB = A$

(2) $A.(A + B) = A$

(3) $A + \overline{A}B = A + B$

(4) $A.(A + B) = AB$

(6) $AB + \overline{A}C + BC = AB + \overline{A}C$

(7) $A + \overline{A} = 1$

(8) $A + O = A$

(9) $A + 1 = 1$

(10) $A \cdot A = A$

(11) $A + A = A$

(12) $A + \overline{A} = 1$

(13) $\overline{\overline{A}} = A$

Q.4. Explain De'Morgans Theorem

Sol. De'Morgan gaver 2 theorms.

The first theorms states that

$$\overline{A + B} = \overline{A}.\overline{B}$$

Proof:

Let X = A+B, the $\overline{X} = \overline{A}.\overline{B}$ has to be proved.

And we must prove

$X - \overline{X} = 0$ and $X + \overline{X} = 1$

$X+\overline{X} = (A+B) + \overline{A}.\overline{B}$. (A+BC = (A+B) (A+C)

$= (A+B+\overline{A}).\ (A+B+\overline{B})$

$= (1+B).\ (A+1)$

$= 1.1$

$= 1$

and

$X.\overline{X} = (A+B).\ (\overline{A}\overline{B})$

$A.\overline{A}\overline{B} + B.\overline{A}.\overline{B}$. (Distributive property)

$(A.\overline{A}).\ \overline{B} + \overline{A}(B.\overline{B})$

$= O.\overline{B}. + \overline{A}.O \ \because\ (X.\overline{X} = O)$

$= 0$ H.P.

De'Morgan's second theorem states that

$$\overline{A.B} = \overline{A} + \overline{B}$$

Proof:

Let $X = A.B$ and $\overline{X} = \overline{A} + \overline{B}$

Then we have to prove that

$X + \overline{X} = 1 \times X.\overline{X} = 0$

$X + \overline{X} = AB + \overline{A} + \overline{B}$

$(\overline{A} + A).(\overline{A} + B) + \overline{B}$

$= 1.(\overline{A} + B) + \overline{B}$

$= A + B + B$

$= \overline{A} + 1$

$= 1$

$X.\overline{X} = AB(\overline{A} + \overline{B})$

$A.\overline{A}.B + A.B.\overline{B}$

$0.B = A.0$

$= 0 + 0$

$= 0$

p p p

Chapter 2

Karnaugh Maps

Q.1. Explain the concept of sum of products and product of sums.

Sol. Logical functions are generally expressed in terms of logical variables. A logical functions can be expressed as

(i) Sum of products (SOP)

(ii) Product of sums (POS)

(i) SOP – The logical sum of 2 or more logical product terms, is called as SOP. Its basically an OR operation of AND operated variables such as:

(i) $Y = AB + BC + AC$

(ii) $Y = AB + \overline{A}C + BC$

(ii) POS: A product of sums exp. is a logical product of 2 or more logical sum terms. Its basically an AND operation of OR operated variables such as:

(i) $Y = (A + B)(B + C)(C + \overline{A})$

(ii) $Y = (A + B + C)(A + \overline{C})$

Q.2. Explain the concept of min terms and max terms.

Sol. A product term containing all the K. variables of the function in either complemented or uncomplemented form is called minterm.

Now, a 2 variable function has 4 possible combinations. Viz. $\overline{A}\overline{B}$, $\overline{A}B$, $A\overline{B}$, AB. These product terms are called min terms. In the min term, a variable appears either in uncomplemented form, if it possess a value 1 or in complemented form if it has a value 0.

Eg. A 3 variable fun has min terms represented as Mo, M_1, M_2…..M_7.

A	B	C	Min terms
0	0	0	$\overline{A}\overline{B}\overline{C}$
0	0	1	$\overline{A}\overline{B}C$
0	1	0	$\overline{A}B\overline{C}$
0	1	1	$\overline{A}BC$
1	0	0	$A\overline{B}\overline{C}$
1	0	1	$A\overline{B}C$
1	1	0	$AB\overline{C}$
1	1	1	ABC

for K variable fun, there would be 2^K-1 min terms.

(ii) Max terms: A sum term containing all K variables of a fun in either complemented or uncomplemented form is called as max term. A 2 variable fun has 4 possible combinations, viz. $A+B$, $A+\overline{B}$, $\overline{A}+B$, $\overline{A}+\overline{B}$. These terms are called max terms.

In a max term, a variable appears either in uncomplemented form if it possess the value O or in complemented form if it contains value 1. The max terms of a 3 variable form is expressed as Mo, M_1, M_2, M_3, M_4, M_5, M_6, M_7.

A	B	C	Max terms
0	0	0	A+B+C
0	0	1	$A+B+\overline{C}$
0	1	0	$A+\overline{B}+C$
0	1	1	$A+\overline{B}+\overline{C}$
1	0	0	$\overline{A}+B+C$
1	0	1	$\overline{A}+B+\overline{C}$
1	1	0	$\overline{A}+\overline{B}+C$
1	1	1	$\overline{A}+\overline{B}+\overline{C}$

Q.3. What are Karnuagh maps and explain them.

Sol. As the no. of variables in a function increase, it becomes more difficulty to simplify the functions The Kaurnaugh map techniques called K- maps provide a systematic method for simplifying the expressions. In this techniques, the info in the truth table or available in the POS or SOP form is represented on the K-Maps. The K map can be used as a modified form of TT. In a n variable K-map, there are 2^n cells. Each all corresponds to one combination of n-variables.

The Karnaugh maps for different variables are shown below:

(a) 2 variable:

A \ B	0	1
0	0	2
1	1	3

(b) 3- variable

C \ AB	00	01	11	10
0	0	2	6	4
1	1	3	7	5

(c) 4-variable

CD \ AB	00	01	11	10
00	0	4	12	8
01	1	5	13	9
11	3	7	15	11
10	2	6	14	10

Eg. The entries in a truth tabled can be represented in K-map given below:

Consider the truth table.

A	B	C	output- XY
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$\therefore$ Now the O/P can be written as:

$$Y = \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C} + ABC$$

$$Y(A,B,C) + M_1 + M_2 + M_4 + M_7$$

The K- map for this would be

C \ AB	00	01	11	10
0	0	1	0	1
1	1	0	1	0

Simplification of the function is based on certain rules. They are as follows:

(1) Constant the K-maps enter the 1's in those cell corresponding to the combinations for whide function value is 1, then enter the O's in the other cell.

(2) Examine the map for 1's that cannot be combined with any other 1 cells and form groups with such single 1.

(3) Next, look for those 1's which are adjacent to only one other 1 and form groups containing only 2 cells and which are not part of any group of 4 or 8 cells. A group of 2 cells is called a pair.

(4) Group the 1's which result in groups of 4 cells but are not part of 8 cells. A group of 4 cells is called quad.

(5) Group the 1's which result in groups of 8 cells. A group of 8 cells is called an octet.

(6) Form more pairs, quads and octets to include there is that have not yet been grouped and use only a minimum no. of group. There can be overlapping of groups if they include common 1's.

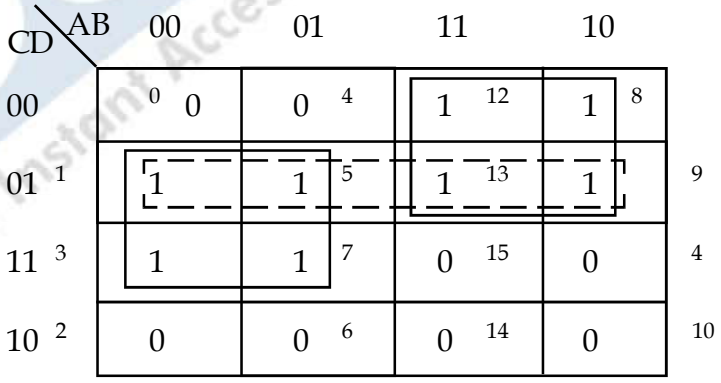
(7) Omit any redundant group.

(8) Form the logical sum of all the terms generated by each group.

Q.4. Simply the following exp. using K-map for the 4-variables A,B,C,D.

$Y = M_1 + M_3 + M_5 + M_7 + M_8 + M_9 + M_{12} + M_{13}$.

Sol. The K map is shown below



Step 1. Construct the K-Map.

Step 2. There are no is which are not adjacent to other 1's.

Step 3. There are no pairs which are not part of any other largen groups.

Step 4. There are 2 quads cells 1, 3, 5, 8, 7 are grouped to form one quad and the second quad is made up of cells 12, 13, 8 & 9. The combinations corresponding to the cells in the first quad are $\overline{A}\overline{B}\overline{C}\overline{D}$, $\overline{A}\overline{B}CD$, $\overline{A}B\overline{C}D$, & $\overline{A}BCD$. In the above group of 4 combinations, the variables $\overline{A}D$ are common in all the cells which B and C appear both in complement and uncomplemented forms. The minimized term for the first quad is $\overline{A}D$, and that of the second quad is $A\overline{C}$.

Step 5. There are no octets.

Step 6. All the 1's have already been grouped.

Step 7. The terms generated by the 2 groups are OR operated together to obtain the expression for Y as:

$$\boxed{Y = A\overline{C} + \overline{A}D}$$

Q.5. What do you understand by "don't care combination"?

Sol. In certain digital systems, some i/p combinations never occur during the process of normal operations because those i/p conditions are guaranteed never to occur. Such i/p combination are known as don't care combination. We don't care what the function O/P is for such combination. These combinations can be plotted on a map to provide further simplification of the functions.

Q.6. Explain the Quine-Mclusky Method.

Sol. This tabulation method is an alternative to the K-map method for the simplification of functions. It was developed by W.V. Quine and E.J. McClusky. It consists of following steps.

(i) To find all the terms (called prime Implicants) that are candidate for inclusion in prime implicant table.

(ii) To select those prime-implicants that give an expression with minimal no. of variables.

(iii) Test for minimal and optimal expressions.

The procedure to be followed to find prime implicants is:

(i) All the min terms are represented by their binary representation.

(ii) All the min terms are classified according to the number of 1's present in its binary representation. All the terms with equal number of 1's present in its binary representation are put. Under 1 section eg. m_1 (0001), M_2 (0010), M_4 (0100) etc. are under 1 section.

(iii) Each term of one section is compared with every term of next section. Only those terms are combined whose binary representation differs in only one bit and a dash is put at the position which differ in 1 bit. The terms which are combined are marked as ticked. This procedure is followed for all the section of terms.

(iv) All the combined terms are their compared further and if the binary equalent representation of terms differ in one bit position, a dash is put at that position. All the terms which have been combined are ticked and checked.

(v) All the terms are finally available as unchecked and unticked are part of final simplified expression.

Eg. Simplify the function

$$F(A, B, C, D) = \Sigma (0, 2, 5, 7, 8, 10, 13, 15)$$

The equivalent binary word for the given min term are :

Decimal digit	Binary word
0	0000
2	0010
5	0101
7	0111
8	1000
10	1010
13	1101
15	1111

The given min terms are divided in different sections in accordance with no. of 1's.

			No. of 1's
Section 0	Mo	0000	0
Section 1	M_2	0010	1
	M_8	1000	
Section 2	M_5	0101	2
	M_{10}	1010	
Section 3	M_7	0111	3
	M_{13}	1101	
Section 4	M_{15}	1111	4

A comparison table is now prepared to find the prime implesants (PI's) which are a part of the minimal simplified exp.

		Step 1		Step 2	
		ABCD		ABCD	ABCD
Section '0':	0	0000√	(0,2)	00—0√	
Section 1:	2	0010√	(0,8)	—000√	(0,2,8,10)—0—0*
	8	1000√	(2,10)	—0101√	(0,8,2,10)—0—0*
Section 2:	5	0101√	(8,10)	10—0√	
	10	10101√	(5,7)	01—1√	
Section 3:	7	0111√	(5,13)	—101√	(5,7, 13,15)—1—1*
	13	1101√	(7,15)	—111√	(5,13, 7,15)—1—1*
Section 4:	15	1111√	(13,15)	11—1√	

From the table, the minimal simplified expression is:

$$F(A,B,C,D) = \overline{B}\,\overline{D} + BD$$

Where $\overline{B}\,\overline{D}$ corresponds to —0—0

And BD corresponds to —1—1

As a final step optimality test table is prepared as shown below :

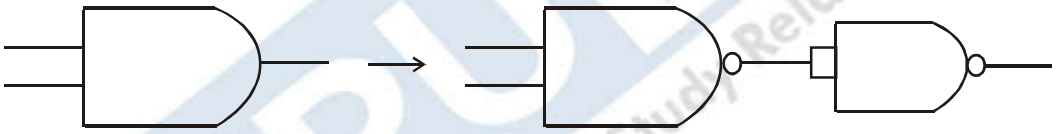
Terms / PI's	0000	0010	1000	0101	1010	0111	1101	1111
–0 –0	√	√	√		√			
–1 –1				√		√	√	√

Since, no column consists of more than 1 tide the expression obtained is optimal one.

Q.7. Why are NAND and NOR gates called universal gates.

Sol. NAND and NOR gates are known as universal gates b'coz any other type of logical gate can be synthesized or implemented using these 2 gates. These gates can be easily realized as multi-input gates on the I.C. chips.

Eg. AND gate can be relized using NAND gate as:



AND NAND + Winter

p p p

Chapter 3

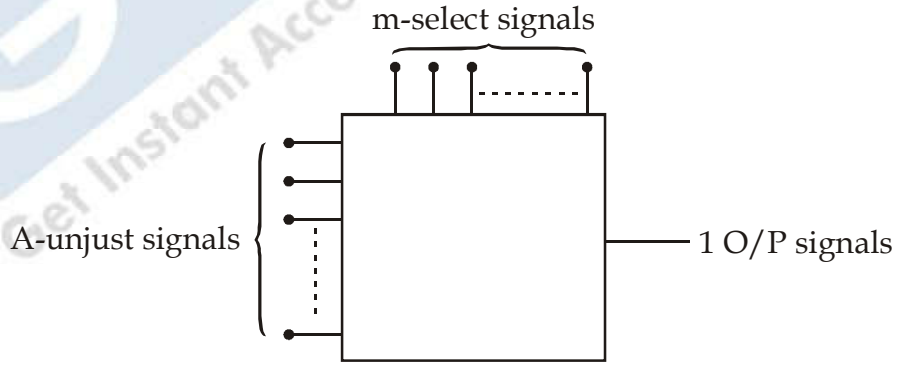
Combinational Circuits

Q.1. What are Combinational Circuits ?

Sol. They are circuits in which output at any time depends upon the combination of the input signals present at that instant only, and does not depend upon the past conditions.

Q.2. What is a multiplexer and explain the multiplexer IC 74150 & IC 74151?

Sol. The term multiplener means "many to one" it means transmitting a large number of info on a single line. A digital (MUX) is a combinational circuit that selects one digital information from several sources and transmits the selected into on a single O/P line.



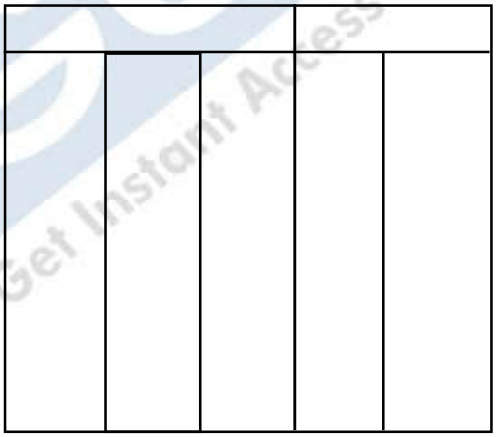
IC74151-8 to 1 Multiplexer: Its an 8- to -1 MUX with 8 data inputs, 3

select input lines (S_2-S_O) and a single output. It also has enable input E and provides both normal and invested O/Ps.

Truth table

Inputs				Outputs	
$\overline{E}$	S_2	S_1	S_0	Y	$\overline{Y}$
1	X	X	X	1	0
0	0	0	0	D_o	$\overline{D}_o$
0	0	0	1	D_1	$\overline{D}_1$
0	0	1	0	D_2	$\overline{D}_2$
0	0	1	1	D_3	$\overline{D}_3$
0	1	0	0	D_4	$\overline{D}_4$
0	1	0	1	D_5	$\overline{D}_5$
0	1	1	0	D_6	$\overline{D}_6$
0	1	1	1	D_7	$\overline{D}_7$

IC-74150-16 to 1 Multiplexer: It's a 16 to -1 TTL multiplexer. It has 16 inputs (D_O-D15), a single O/P and 4 select pins. Pins 1 to 8 and 16 to 23 are i/p pins and the pins 11, 13, 14 and 15 are the select i/p's. $S_3S_2S_O$. Pin 10 is the O/P and it equals the complement of the selected data input. Truth table.

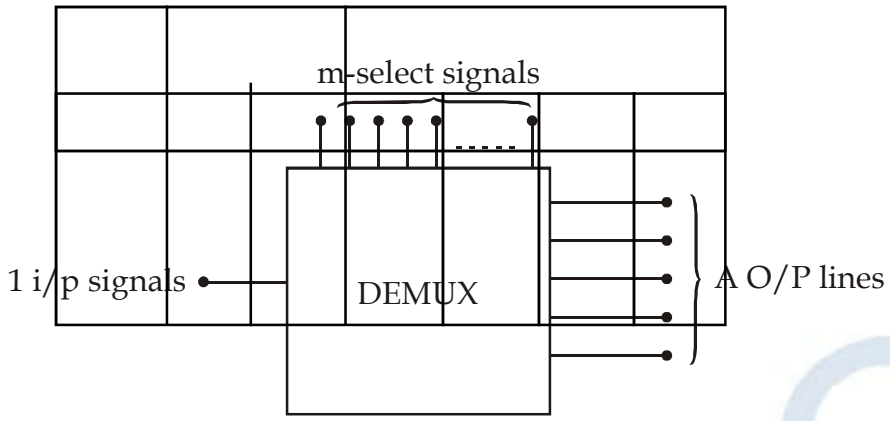


Select Pine			Output	
S_3	S_2	S_1	S_0	Y
0	0	0	0	$\overline{D}_o$
0	0	0	1	$\overline{D}_1$
0	0	1	0	$\overline{D}_2$
0	0	1	1	$\overline{D}_3$
0	1	0	0	$\overline{D}_4$
0	1	0	1	$\overline{D}_5$
Select Pine			**Output**	
S_3	S_2	S_1	S_0	Y
0	1	1	0	D_6
0	1	1	1	D_7
1	0	0	0	D_8
1	0	0	1	D_9
1	0	1	0	D_{10}
1	0	1	1	D_{11}
1	1	0	0	D_{12}
1	1	0	1	D_{13}
1	1	1	0	D_{14}
1	1	1	1	D_{15}

Q.3. What are Demultiplexers. Explain IC- 74154 ?

Sol. The word "demultiplexer means one into many denultiplexing is the process of taking info from i/p and transmitting the same over one of several O/p's.

A demultiplexer is a logic circuit that receives information on a single i/p and transmits the same into over one of several (2^n) O/P lines.



A 1 – to 4 demultiplexer has the following truth table.

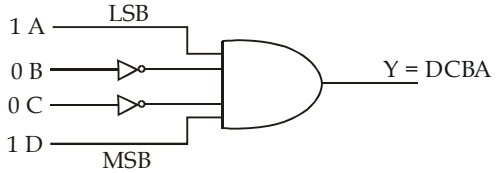
Data Input	Select input		Outputs			
D	**S_1**	**S_0**	**Y_3**	**Y_2**	**Y_1**	**Y_0**
D	0	0	0	0	0	D
D	0	1	0	0	D	0
D	1	0	0	D	0	0
D	1	1	0	0	0	0

IC-74154 demultiplex is a 1- to -16 demux with single input, 16 active low inputs 14 select inputs.

Q.4. What are decoders ? Explain IC-74139.

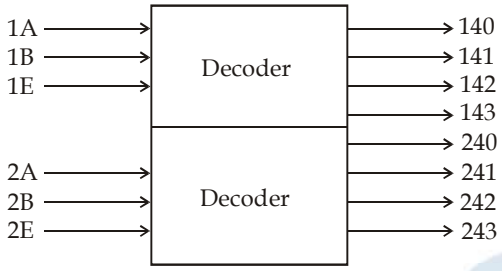
Sol. A decoder is similar to demultiplexer but without any data input. Most digital systems require decoding of the data. A decoder is a logic circuit that converts and n-bit binary i.p code (dta) into 2^n O/P lines such that each i/p line will be activated for only 1 of the possible combination of i/ps.

In a basic binary decoder an AND gate can be used as the basic decoding element. For eg, if the input binary no. is 1001, then, to make all the i/ps to the AND gate high, the 2 middle bits are inverted as shown.



Some decoders have one or more enable i/p's which are used to control the operation of the decoder.

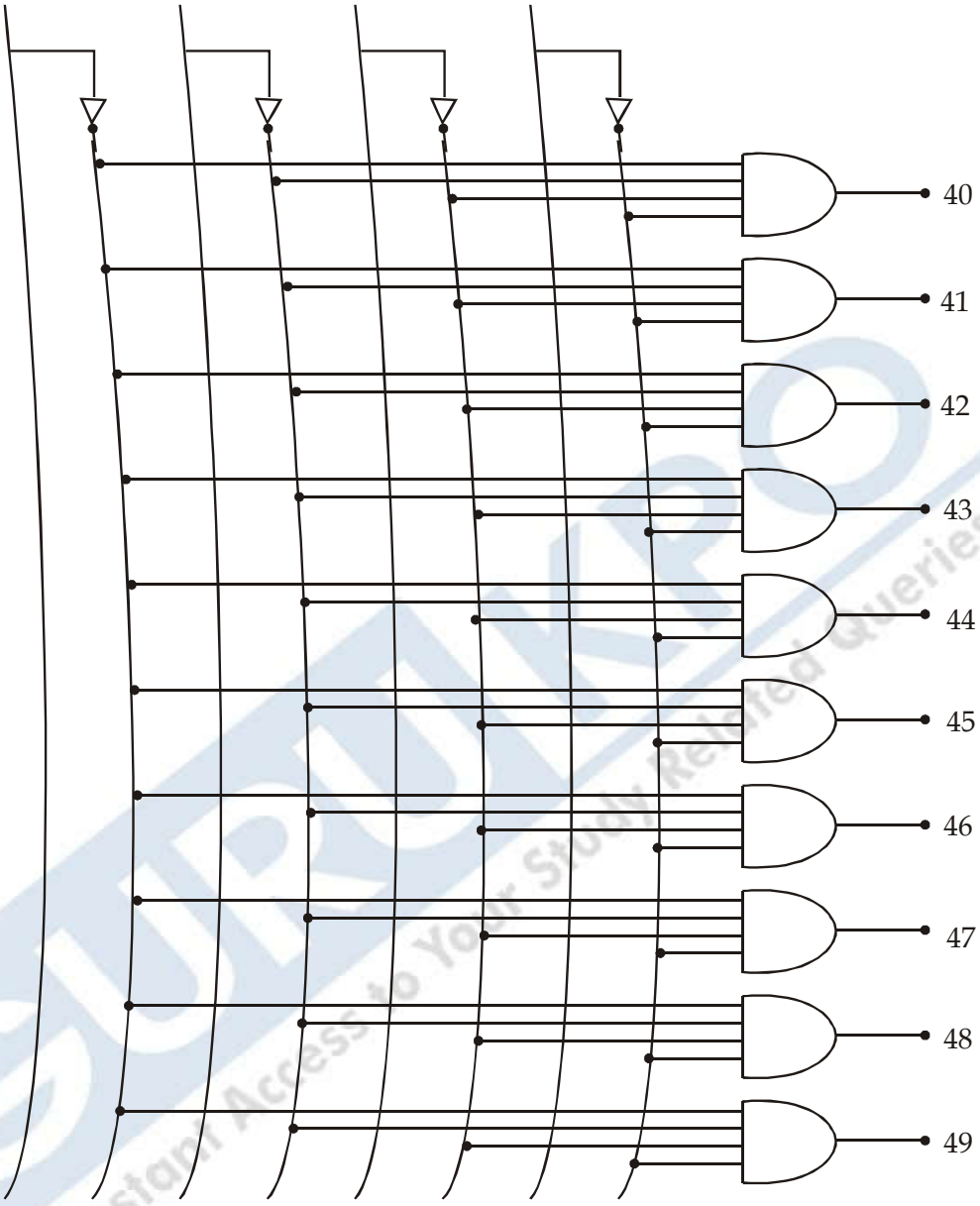
IC-74139 is a Dual 2- to 4 Decoder. It consists of 2 individual 2 – to – 4 decoders in a single package. Each decoder has 2 i/p's, 4 active low O/P's and one active low enable i/p. This active low enable i/p can be used as the data i/p in demultiplening applications.



Q.5. Explain about BCD to Decimal decoder and IC-7445.

Sol. A decoder that takes a 4-bit BCD as the input code and produces 10 outputs corresponding to the decimal digits is called a BCD to decimal decoder.

Diagram is as shown.



Here, each input goes HIGH when its corresponding BCD code is applied at its i/p.

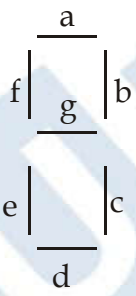
IC-7445 is BCD to Decimal decoder/driver. The term driver is added to its description because this IC has open collector O/P that can operate

at higher current, and voltage limits than a normal TTL O/P.

Q.6. Explain about BCD to 7- segment decoder/Driver.

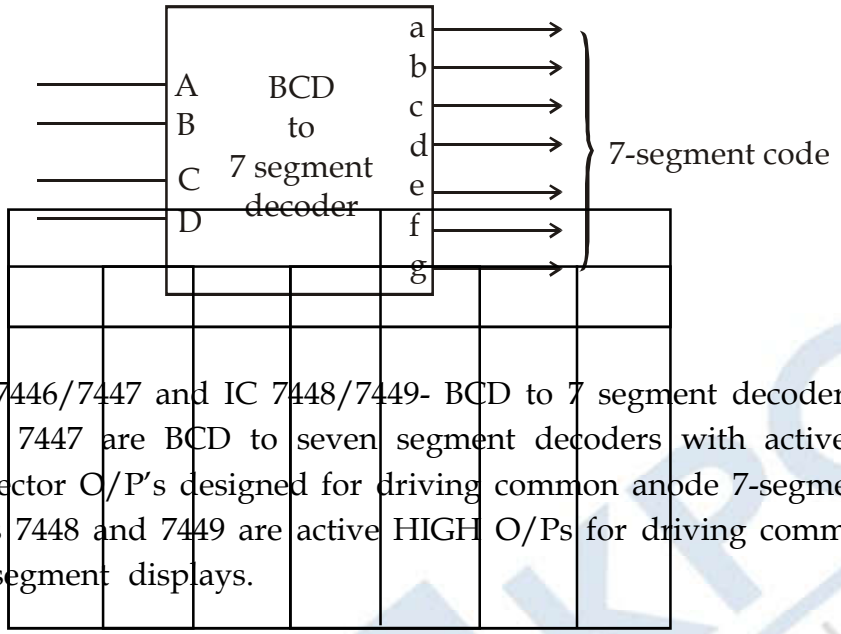
Sol. A seven segment display is normally used for displaying any one of the decimal digits 0 through 9. A BCD- to 7 segment decoder accepts a decimal digit in BCD and generates. The corresponding seven segment code.

The Figure below shows a seven-segment display



The figure shows a seven-segment display composed of 7-segments. Each segment is made up of a LED's. The letters a,b,c,d,e,f, and g run clockwise from top of each segment. For eg., to display 1, the segments bLC have to be illuminated, to display 0, the segments a, b, c, d, e 8 f have to be illuminated.

The decoder can be designed suing logic gates a block diagram of BCD-to – 7 segment decoder with 4 BCD inputs (A, B, C & D) and seven outputs. [a, b, c, d, e, f, g].

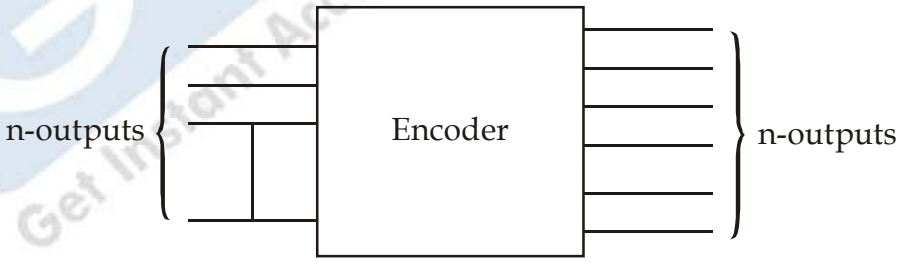


IC 7446/7447 and IC 7448/7449- BCD to 7 segment decoders: IC 74468 and 7447 are BCD to seven segment decoders with active low open collector O/P's designed for driving common anode 7-segment displays IC's 7448 and 7449 are active HIGH O/Ps for driving common cathode 7- segment displays.

Q.7. What are encoders and explain decimal to BCD- encoders ?

Sol. An encoder is a digital circuit that performs, the inverse operation of a decoder. Hence, the opposite of decoding process is called encoding process. It converts an active i/p signal into coded O/P signal.

It has n i/p lines, only one of which is active at any time and m O/P lines. It encodes one of the active i/ps to a coded binary O/P with m bits.



Decimal to BCD Encoder: It has 10 inputs corresponding to 10 decimals (0 to 9) and 4 O/P's (A,B,C,D) representing the BCD value of i/p decimal

digit.

Q.8. Explain about priority encoder.

Sol. A priority is an encoder that includes the priority function. The operation of the priority encoder is such that if 2 or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence. The truth table is shown below:

Inputs				Outputs		
D_0	D_1	D_2	D_3	Y_2	Y_1	Y_0
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

Q.9. What are parity checkers.

Sol. When digital data is transmitted from one location to another, its necessary to know at the receiving end whether the received data us free operons. A simple form of error detection is by adding an entra bit to the transmitted word. This additional bit is known as parity bit and detects errors.

There are 2 types of parity bits, even parity and odd parity

If an input has even no. of I's, its even parity else it is odd parity.

The circuit for generations parity bits and checking the parity of a given word can be designed using gates XOR gates are ideal for checking the parity of a binary number because they produce an O/P when the i/p has an odd number of 1's. Therefore, an even parity input to an XOR gate produces a low O/P, while an odd parity i/p produces a high O/P.

Q.10. Explain about Counters?

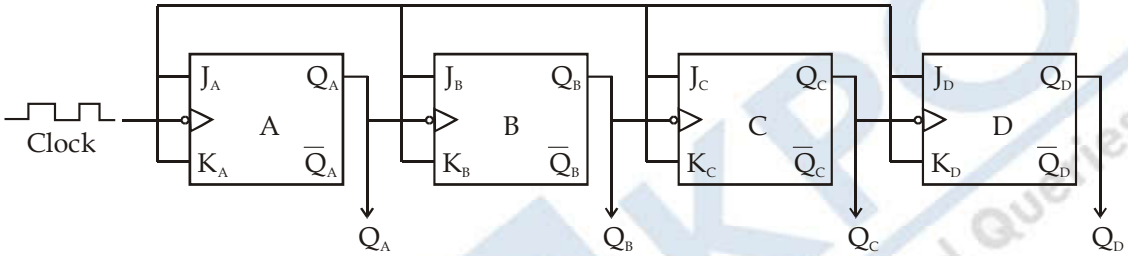
Sol. A counter is a sequential circuit consisting of a set of flip flops connected in a suitable manner to count the sequences of the I/P pulses presented

to it in digital form. Counters are of 2 types.

(1) Asynchronous counters

(2) Synchronous counters

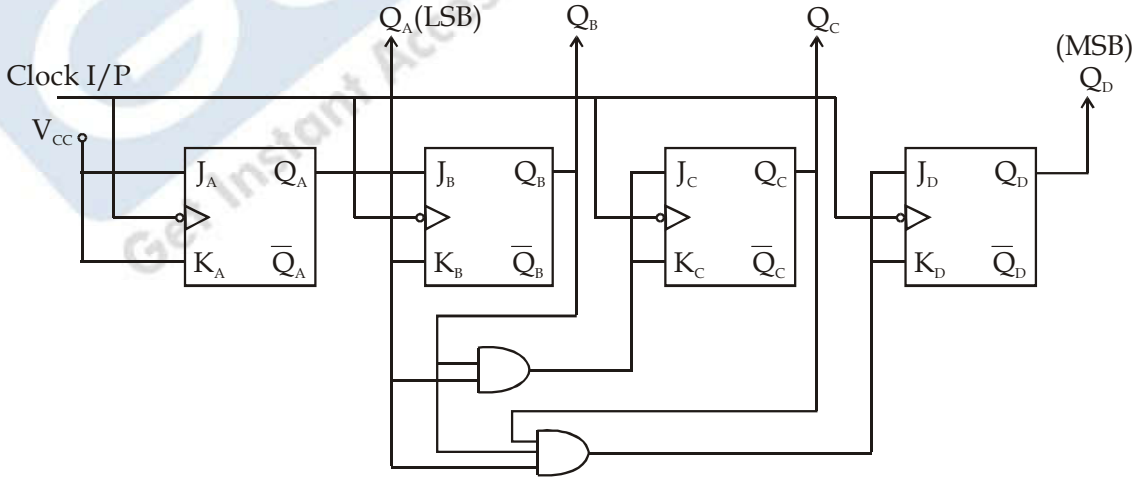
(1) Asynchronous counters: In this counter all the flip flops are not under the control of a single clock. Here, the clock pulse is applied to the first flip-flop, i.e. the least significant bit stage of the counter, and the successive flip flop is triggered by the O/P of previous flip-flop and thus the counter has a cumulative setting time. As the trigger moves through the flip-flops like a ripple, its also called as ripple counter.



A binary ripple counter is constructed using clocked JK-flip flops.

(2) Synchronous counter: It has higher speed of operation than ripple counter and clock pulses are applied to all flip and flops simultaneously.

A 4-bit synchronous counter with parallel is given below. In this, the clock inputs of all the flip-flops are connected together so that the i/p clock signal is applied simultaneously to each flip flop. Also, only the LSB flip flop A has its J and K i/p's connected permanently to Vc, while the J& K i/ps of the other flip-flops are driven A-B by some combination of flip-flop outputs.



In a synchronous counter, all flip-flops change their states simultaneously, is, they are synchronized with the negative transition of the i/p clock signal.

Q.11. Explain about up/down counter.

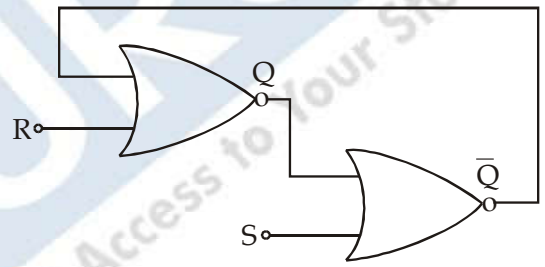
Chapter 4

Sequential Circuits

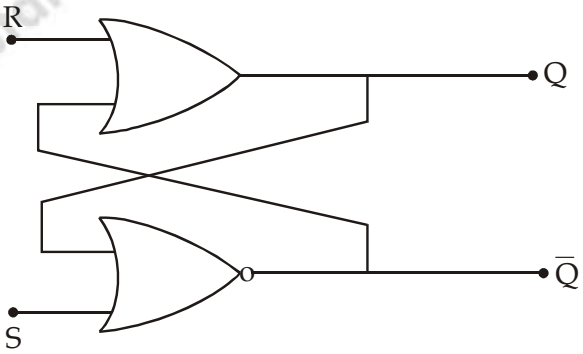
Q.1. What an different types of Flip-Flops ?

Ans. The following types of flip-flops are listed below.

(1) S-R Flip-Flop: A SR flip flop can be realized connecting 2 NOR gates as shown below.



It can be also drawn as:



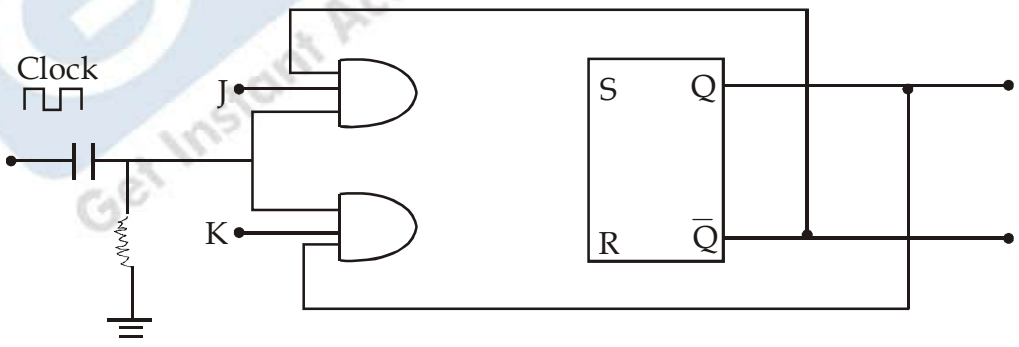
Q is O/P of the flip-flop. Q is the complement of the O/P. Thus a high on S (Keeping R = O) i/p will make. Q =). Q is one of this i/p's to the upper NOR gate. As both i/p (R & Q) of the upper NOR gate an now low, its output Q until be high. Thus, the flip-flop stores binary bit 1 when 8 is made high. Even of the set i/p S is removed, the O/P Q will remain 1 because Q is one of the i/ps of the lower NOR gate. 111^{ly}, when reset input R is mad, high keeping S = 0, Q will become low.

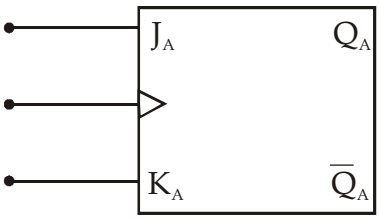
Truth Table for S-R Flip-Flop

R	S	Q	Action
0	0	Hard Value	No changes
0	1	1	Set
1	0	0	Reset
1	1	-	Invalid condition

When both S & R are made high simultaneously, it will make the O/P's of both NOR gates low which is against base definition of a flip-flop.

J-K Flip-Flops: In an S-R flip flop, the state of the O/P is unpredictable. When S= R-1. A J-K flip flop allows inputs J-K = 1. In this situation, this states of the O/P is changed. This complement of the promotes state is available at the output terminal.





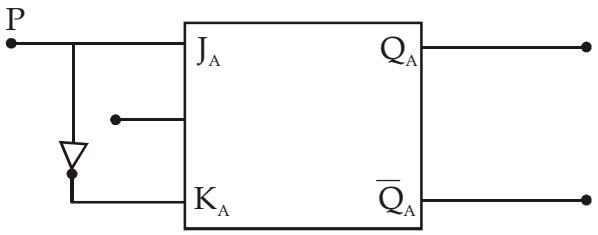
When J and K both an O, the O/P's of the AND gates will be low, i.e., S & R an both low. When S & R are both low, then will be no change in the O/P State.

When J = O and K = 1, the O/P of this upper AND gate, i.e. S becomes low, its not possible to set the flip-flop. As K=1, the O/P of the lower and AND gate, is R will the high if the other input of the gate Q is high.

The truth table is shown below:

	Inputs		Ouputs
ChK	J	k	Q_{n+1}
X	0	0	Qn (No changes, remains is last state)
1	1	0	1
1	0	1	0
1	1	1	Qn (Toggle)

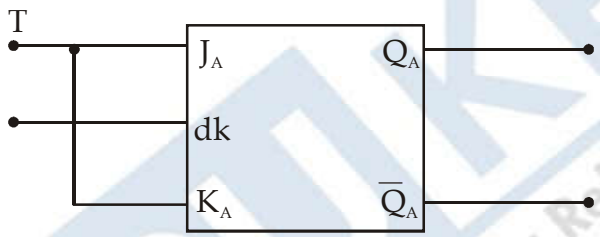
D-Flip Flops: An S-R flip flop has 2 inputs, S & R. To store 1, a high S and low R an required. To stone O, a high R below S are needed. Thus, 2 signals an to be generated to draw an S-R flip flop. A D-flip-flop can be realized using an S-R flip- Flop as shown.



The truth table for D flip-flop is shown below:

Clk	D Input	Q_{n+1}
0	X	Qn (last state)
1	1	1
1	0	0
1	X	Q_n (last state)

T-Flip- Flop: A T-Flip-Flop acts a toggle switch toggle means to switch over to the opposite state. It can be realized using a I-K flip flop by making T = I = K =1, as shown in the figure below:

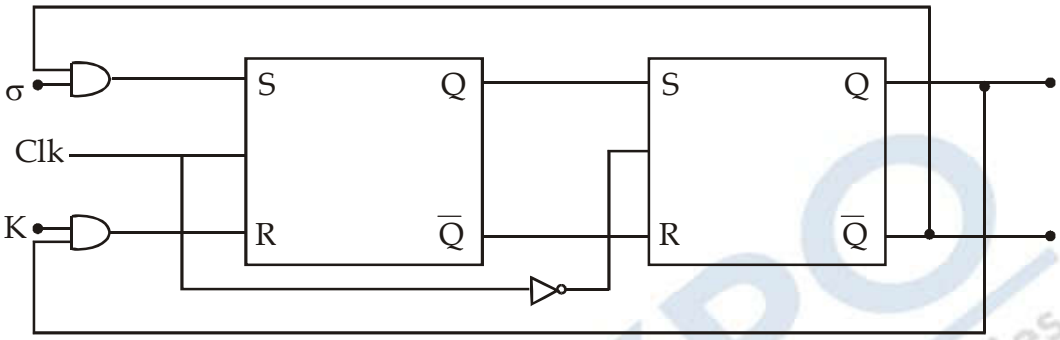


Truth Table

Input	Output
T	Q_{n+1}
O	Q_n
1	Q_n

Master slave flip-flop: It consist of 2 clocked S-R flip flops. One is called master and second is called slave. When the clock is high, the master is active and slave inactive. The master sets or resets according to the state of the i/p signals as the slave is inactive during this period, its O/P remains steady at the previous state. When the clock goes low, the master is inactive and the slave is active. The slave sets or resets according

to its i/ps. The final O/P Q of a master-slave flip flop is O/P of the slave.



p p p